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申请人：松下电器产业株式会社

发明创造名称：光盘装置

第一次审查意见通知书

1. ☑应申请人提出的实审请求，根据专利法第35条第1款的规定，国家知识产权局对上述发明专利申请进行实质审查。
   ☐根据专利法第35条第2款的规定，国家知识产权局决定自行对上述发明专利申请进行审查。
2. ☑申请人要求以其在：
   JP　专利局的申请日　2002年　10月　23日为优先权日，
   　专利局的申请日　年　月　日为优先权日，
   　专利局的申请日　年　月　日为优先权日，
   　专利局的申请日　年　月　日为优先权日，
   　专利局的申请日　年　月　日为优先权日。
   ☑申请人已经提交了经原申请国受理机关证明的第一次提出的在先申请文件的副本。
   ☐申请人尚未提交经原申请国受理机关证明的第一次提出的在先申请文件的副本，根据专利法第30条的规定视为未提出优先权要求。
3. ☐经审查，申请人于：
   年　月　日提交的　不符合实施细则第51条的规定；
   年　月　日提交的　不符合专利法第33条的规定；
   年　月　日提交的
4. 审查针对的申请文件：
   ☐原始申请文件。　☑审查是针对下述申请文件的
   申请日提交的原始申请文件的权利要求第　1-10　项、说明书第　1-14　页、附图第　1-8，10　页；
   2003年　12月　31日提交的权利要求第　项、说明书第　页、附图第　9　页；
   年　月　日提交的权利要求第　项、说明书第　页、附图第　页；
   年　月　日提交的权利要求第　项、说明书第　页、附图第　页；
   年　月　日提交的说明书摘要，　年　月　日提交的摘要附图。
5. ☐本通知书是在未进行检索的情况下作出的。
   ☑本通知书是在进行了检索的情况下作出的。
   ☑本通知书引用下述对比文献(其编号在今后的审查过程中继续沿用)：

编号	文件号或名称	公开日期（或抵触申请的申请日）
1	CN1280361A	2001-1-17

6. 审查的结论性意见：
   ☐关于说明书：
   ☐申请的内容属于专利法第5条规定的不授予专利权的范围。

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（注：凡寄给审查员个人的信函不具有法律效力）

☐说明书不符合专利法第 26 条第 3 款的规定。
☐说明书不符合专利法第 33 条的规定。
☐说明书的撰写不符合实施细则第 18 条的规定。
☐________

☑关于权利要求书：
☐权利要求________不具备专利法第 22 条第 2 款规定的新颖性。
☑权利要求1-3, 7, 8, 10不具备专利法第 22 条第 3 款规定的创造性。
☐权利要求________不具备专利法第 22 条第 4 款规定的实用性。
☑权利要求___9___属于专利法第 25 条规定的不授予专利权的范围。
☐权利要求________不符合专利法第 26 条第 4 款的规定。
☐权利要求________不符合专利法第 31 条第 1 款的规定。
☐权利要求________不符合专利法第 33 条的规定。
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☐权利要求________不符合专利法实施细则第 13 条第 1 款的规定。
☐权利要求________不符合专利法实施细则第 20 条的规定。
☐权利要求________不符合专利法实施细则第 21 条的规定。
☐权利要求________不符合专利法实施细则第 22 条的规定。
☐权利要求________不符合专利法实施细则第 23 条的规定。
☐________

上述结论性意见的具体分析见本通知书的正文部分。

7. 基于上述结论性意见，审查员认为：
☐申请人应按照通知书正文部分提出的要求，对申请文件进行修改。
☑申请人应在意见陈述书中论述其专利申请可以被授予专利权的理由，并对通知书正文部分中指出的不符合规定之处进行修改，否则将不能授予专利权。
☐专利申请中没有可以被授予专利权的实质性内容，如果申请人没有陈述理由或者陈述理由不充分，其申请将被驳回。
☐________

8. 申请人应注意下述事项：

(1) 根据专利法第 37 条的规定，申请人应在收到本通知书之日起的肆个月内陈述意见，如果申请人无正当理由逾期不答复，其申请将被视为撤回。
(2) 申请人对其申请的修改应符合专利法第 33 条的规定，修改文本应一式两份，其格式应符合审查指南的有关规定。
(3) 申请人的意见陈述书和/或修改文本应邮寄或递交国家知识产权局专利局受理处，凡未邮寄或递交给受理处的文件不具备法律效力。
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9. 本通知书正文部分共有___2___页，并附有下述附件：
☑引用的对比文件的复印件共___1___份___3___页。☐________

朱朔印

审查员：朱朔(3612)
2006 年 2 月 27 日

审查部门 通信审查部

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第一次审查意见通知书正文

申请号：2003101025296

本申请涉及一种光盘装置。经审查，现提出如下的审查意见。

1. 权利要求1请求保护一种光盘装置，对比文件1（CN1280361A）也公开了一种用于跟踪误差检测的装置，并具体公开了以下技术特征（参见说明书第3页第8行一第28行，附图1）：四单元式光学检测组件102（相当于该权利要求中的光检测器），高通滤波器106a和106b（相当于该权利要求中将各再生信号中频率成分降低的滤波器），相位比较器110（相当于该权利要求中的相位差检测器），输出跟踪误差信号的低通滤波器LPF112（相当于该权利要求中的信号生成部），由此可见，对比文件1已经公开了权利要求1中的大部分技术特征。

权利要求1与对比文件1的区别在于，权利要求1具有光学系和根据跟踪误差信号生成控制信号的控制部，并据此控制光照射位置。但是对本领域技术人员来说，照射光盘的光学系统是光盘装置中必不可少的公知装置，而根据所得的跟踪误差信号控制光照射位置的控制部也是本领域常用的公知装置，本领域技术人员很容易想到在对比文件1的基础上结合上述公知常识得到权利要求1所要求保护的技术方案，这种结合也没有产生预料不到的技术效果，因此该权利要求1不具备突出的实质性特点和显著进步，不具备专利法第22条第3款所规定的创造性。

2. 权利要求2和3中的附加技术特征均是本领域公知常识，所述光学系、根据控制信号控制透镜位置、以及滤波器去除频率成分均是本领域常用的技术手段，因此上述权利要求2和3也不具备突出的实质性特点和显著进步，在其各自引用的权利要求不具备创造性时，该权利要求2和3也不具备专利法第22条第3款所规定的创造性。

3. 权利要求7中的附加技术特征是本领域公知常识，因此该权利要求7也不具备突出的实质性特点和显著进步，在其引用的权利要求1不具备创造性时，该权利要求7也不具备专利法第22条第3款所规定的创造性。

4. 权利要求8请求保护一种跟踪控制方法，对比文件1（CN1280361A）也公开了一种用于跟踪误差检测的方法，并具体公开了以下技术特征（参见说明书第3页第8行一第28行，附图1）：四单元式光学检测组件102生成光学检测信号A、B、C、D（相当于该权利要求中接收反射光的步骤以及生成对应的多个再生信号的步骤），高通滤波器106a和106b增强高频分量（相当于该权利要求中将各再生信号中频率成分降低的步骤），相位比较器110检测相位差（相当于该权利要求中的检测相位差的步骤），

低通滤波器LPF112输出跟踪误差信号（相当于该权利要求中的生成跟踪误差信号的步骤），由此可见，对比文件1已经公开了权利要求8中的大部分技术特征。

权利要求8与对比文件1的区别在于，权利要求8具有在光盘上照射光的步骤和根据跟踪误差信号生成控制信号，并据此控制光照射位置的步骤。但是对本领域技术人员来说，光学系统照射光盘是本领域必不可少的公知步骤，而根据所得的跟踪误差信号生成控制信号控制光照射位置也是本领域常用的技术手段，本领域技术人员很容易想到在对比文件1的基础上结合上述公知常识得到权利要求8所要求保护的技术方案，这种结合也没有产生预料不到的技术效果，因此该权利要求8不具备突出的实质性特点和显著进步，不具备专利法第22条第3款所规定的创造性。

5. 权利要求9请求保护一种跟踪控制程序，是一种智力活动的规则和方法，即权利要求9属于专利法第25条第1款第（二）项所述的智力活动的规则和方法的范围，因此不能被授予专利权。

6. 权利要求10请求保护一种芯片电路，对比文件1（CN1280361A）也公开了一种用于跟踪误差检测的装置，并具体公开了以下技术特征（参见说明书第3页第8行一第28行，附图1）：四单元式光学检测组件102（相当于该权利要求中的光检测器），高通滤波器106a和106b（相当于该权利要求中将各再生信号中频率成分降低的滤波器），相位比较器110（相当于该权利要求中的相位差检测电路），输出跟踪误差信号的低通滤波器LPF112（相当于该权利要求中的信号生成电路），由此可见，对比文件1已经公开了权利要求10中的大部分技术特征。

权利要求10与对比文件1的区别在于，权利要求10具有光学系和根据跟踪误差信号生成控制信号的控制电路，并据此控制光照射位置的芯片电路。但是对本领域技术人员来说，照射光盘的光学系统是光盘装置中必不可少的公知装置，而根据所得的跟踪误差信号生成控制信号的控制电路和控制光照射位置的芯片电路也是本领域常用的公知装置，本领域技术人员很容易想到在对比文件1的基础上结合上述公知常识得到权利要求10所要求保护的技术方案，这种结合也没有产生预料不到的技术效果，因此该权利要求10不具备突出的实质性特点和显著进步，不具备专利法第22条第3款所规定的创造性。

综上所述，申请人应当在本通知书指定的答复期限内对本通知书提出的问题进行答复，并修改专利申请文件，否则本申请将难以获得批准。申请人对申请文件的修改应当符合专利法第33条的规定，不得超出原说明书和权利要求书记载的范围。

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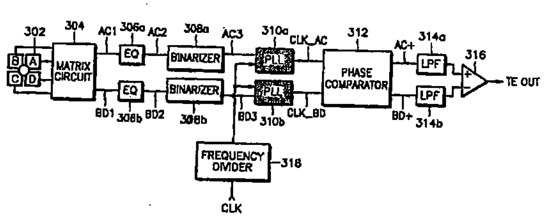
(54) **Method and apparatus for tracking error detection in optical disk driver**

(57) A improved method and apparatus for tracking error detection capable of enhancing accuracy in a tracking error detection with introduction of a phase locked loop (PLL) into a conventional differential phase detection tracking error (DPD TE) method are described. The tracking error detecting apparatus for producing a tacking error signal as a difference signal of optical detection signals generated from more than two optical detectors (302) positioned along a diagonal line from a track center includes binarizers (308) for binarizing each of outputs of the optical detectors (302), PLLs (310) for generating clock signal synchronized with each of the output of the binarizers (308), a phase difference detector (312) for detecting a phase difference between the synchronized signals output from the PLLs (310), and low-pass filters (314) for filtering the output of the phase difference detector to output the result as the tracking error signal. The tracking error detecting apparatus is capable of generating a tracking error signal which is not dependent on the lengths of pits or marks recorded on an optical disk, so that the reliability of a tracking error signal can be enhanced.

FIG. 3



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EP 1 067 525 A2

Description

[0001] The present invention relates to a method and apparatus for tracking error detection and more particularly, to an improved method and apparatus for tracking error detection in which a phase locked loop (PLL) is introduced into a conventional differential phase detection tracking error (DPD TE) method to increase the accuracy of tracking error detection.

[0002] In a conventional DPD TE method, phase differences are generated on the edges of pits or marks of an optical disk. The length of pits or marks recorded on an optical disk lies in various ranges. For example, in the case of digital versatile disk-ROM (DVD-ROM), a length ranges from 3T to 14T where T is the duration of a channel clock of the disk. If there are a lot of pits or marks having a short length, phase difference detection can be performed many times, thereby enhancing the reliability of a tracking error signal derived therefrom. Conversely, if there are more pits or marks having a long length, the number of times phase difference detection may be done is reduced, thereby degrading the reliability of a tracking error signal. Further, a spectrum component, according to a modulation method of signal recorded on a disk, is closely related to outputs of AC+ and BD+, and a low-frequency component of the spectrum acts on noise with regard to a tracking error signal which is used for following and determining the position of a tracking center.

[0003] According to a conventional DPD TE method, phase difference detection is supposed to be made from pits or marks at one time, so that the gain and characteristics of a detected signal deteriorate if the signal of pits or marks is adversely affected by defects or the like. In addition, as the track density of an optical disk increases, the magnitude and gain of a tracking error signal according to the conventional DPD TE method decrease. Thus, the conventional DPD TE method has a disadvantage in that it is difficult to precisely control tracking in a high- density track structure.

[0004] With a view to solve or reduce the above problems, it is an aim of embodiments of the present invention to provide a method of improving the accuracy of a tracking error detection with the introduction of a phase locked loop (PLL) into a conventional differential phase detection tracking error (DPD TE) method.

[0005] It is another aim of embodiments of the present invention to provide an apparatus using the above method.

[0006] According to a first aspect of the present invention, there is provided a tracking error detecting method for producing a tracking error signal as a difference signal of optical detection signals generated from more than two optical detectors positioned along a diagonal line from a track center, the method comprising the steps of: binarization for binarizing each of the outputs of the optical detectors; phase locking for generating clock signals synchronized with each of the outputs obtained by the binarization; phase difference detection for detecting a phase difference between the synchronized clock signals output from the phase locking; and low-pass filtering for filtering the output of the phase difference detection to output the result as the tracking error signal.

[0007] According to a second aspect of the invention, t here is provided a tracking error detecting apparatus for producing a tracking error signal as a difference signal of optical detection signals generated from more than two optical detectors positioned along a diagonal line from a track center, the apparatus comprising: binarizers for binarizing each of the outputs of the optical detectors; phase locked loops for generating clock signals synchronized with each of the outputs of the binarizers; a phase difference detector for detecting a phase difference between the synchronized clock signals output from the phase locked loops; and a low-pass filter for filtering the output of the phase difference detector to output the result as the tracking error signal.

[0008] The apparatus preferably comprises equalizers for reinforcing the high-frequency components of the outputs of the optical detectors to output the result to the binarizers.

[0009] Preferably, the equalizers remove low-frequency components of a spectrum from the outputs of the optical detectors, according to a recording modulation method.

[0010] Preferably, a clock signal provided to the phase locked loops is a channel clock signal.

[0011] The tracking error detecting apparatus may further comprise a frequency divider for dividing the frequency of the channel clock signal by n (n=2,3,4,...) to output the result to the phase locked loops when the phase of an output signal is inverted.

[0012] The phase difference detector may generate a first phase difference signal indicating that a first synchronized clock signal output from the phase locked loops leads a second synchronized clock signal output from the phase locked loops, and a second phase difference signal indicating that the second synchronized clock signal leads the first synchronized clock signal, and wherein the low-pass include first and second low-pass filters for filtering the first and second phase difference signals, respectively.

[0013] The tracking error detecting apparatus may further comprise a differential amplifier for generating a tracking error signal corresponding to a difference signal of the outputs of the first and second low-pass filters.

[0014] According to another aspect of the invention, there is provided a tracking error detecting apparatus for producing a tracking error signal as a difference signal of optical detection signals generated from two optical detectors disposed at the outside of the track center of a three-section optical detection unit, the apparatus comprising: for binarizing each of the outputs of the two optical detectors; a phase difference detector for detecting a phase difference between the outputs of the bina-

rizers; and a low-pass filter for filtering the output of the phase difference detector to output the result as the tracking error signal.

[0015] The tracking error detecting apparatus may further comprise phase locked loops coupled to the binarizers and the phase difference detector, which are for generating clock signals synchronized with each of the outputs of the binarizers to output the synchronized signals to the phase difference detector, wherein the phase difference detector detects a phase difference between the synchronized signals output from the phase locked loops.

[0016] For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings in which:

Figure 1 is a block diagram of a tracking error detecting apparatus according to a conventional differential phase detection tracking error (DPD TE) method;

Figure 2 is a wave form diagram showing the operation of the apparatus shown in Figure 1;

Figure 3 is a block diagram of a first preferred embodiment of a tracking error detecting apparatus according to the present invention;

Figure 4 is a wave form diagram showing the operation of the apparatus shown in Figure 3;

Figure 5 is a block diagram of a second preferred embodiment of a tracking error detecting apparatus according to the present invention;

Figure 6 is a block diagram of a third preferred embodiment of a tracking error detecting apparatus according to the present invention;

Figure 7 is a block diagram of a fourth preferred embodiment of a tracking error detecting apparatus according to the present invention;

Figure 8 is a graph of gain versus frequency for the equalizers shown in Figure 3 and 5-7;

Figure 9 is a graph showing the result of comparing a tracking error signal generated by a tracking error detecting apparatus according to embodiments of the present invention, with a tracking signal generated by a conventional DPD TE method; and

Figure 10. is a graph showing the characteristic of gain of tracking error signals generated by a tracking error detecting apparatus according to the present invention and a conventional DPD TE method.

[0017] Referring to Figure 1 which shows the configuration of a tracking error detecting apparatus according to a conventional differential phase detection tracking error (DPD TE) method, The apparatus shown in Figure 1 includes a four-section optical detection unit 102, a matrix circuit 104, high-pass filters (HPFs) 106a and 106b, comparators 108a and 108b, a phase comparator 110, and a low-pass filter (LPF) 112. The apparatus detects a phase difference between the signals output from the four-section optical detection unit 102 to determine the position of a laser spot. If the laser spot deviates from a track center, then it results in a time delay or a phase difference between A+C and B+D signals. Thus, a tracking error signal is generated by detecting the time delay between those signals.

[0018] Specifically, the matrix circuit 104 for adding optical detection signals A and B, and C and D, which are positioned along a diagonal line among the outputs (A, B, C and D) of the four-section optical detection unit 102, turns the outputs AC1 and BD1 into A+C and B+D, respectively. The HPFs 106a and 106b for reinforcing the high-frequency components of AC1 and BD 1 provided from the matrix circuit 104 differentiate AC 1 and BD 1, and output the results, i.e., AC2 and BD2 to the comparators 108a and 108b. The comparators 108a and 108b for binarizing each of AC2 and BD2 provided from the HPFs 106a and 106b, compare AC2 and BD2 with a predetermined level (a ground level in Figure 1) to output the results, i.e., AC3 and BD3 to the phase comparator 110.

[0019] The phase comparator 110 for detecting a phase difference between AC3 and BD3 provided from the comparators 108a and 108b compares the phases of AC3 and BD3 to output the results, i.e., AC+ and BD+ to the LPF 112. In this case, AC+ is a phase difference signal generated when AC3 leads BD3 in phase, while BD+ is a phase difference signal generated when BD3 leads AC3 in phase. The LPF 112 for filtering AC+ and BD+ input from the phase comparator 110 outputs the result as a tracking error signal.

[0020] Figure 2 is a wave form diagram illustrating operation of the apparatus shown in Figure 1. In Figure 2, showing the case in which AC3 leads BD3 in phase, the wave forms of AC3, BD3, AC+ and BD+ signals are illustrated sequentially from the top. As shown in Figure 2, it can be found that if a laser spot deviates by a predetermined amount there exists a phase difference between AC3 and BD3 which is in turn reflected into AC+ and BD+. If AC3 leads BD3 in phase, a tracking error signal is greater than a predetermined central value, but in the opposite case, it is less than the predetermined central value. The degree to which a tracking error signal deviates from the central value corresponds to the distance by which the laser spot is departed from the track center.

[0021] The phase comparator 110 of the apparatus shown in Figure 1 detects a phase difference at a rising or falling edge of AC3 and BD3. The rising or falling edges of AC3 and BD3 correspond to the edges of pits or marks recorded on an optical disk. In other words, the apparatus shown in Figure 1 detects a phase difference once on every edge of pits and marks recorded on an optical disk. Thus, as the number of pits or marks increases, the reliability of a tracking error signal increases, and as the number of pits or marks decreases, the reliability of the signal decreases. If pits or marks are affected by defects of an optical disk or other factors, the gain and characteristics of a tracking error signal become worse. A spectrum component according to a recording modulation method is closely connected with AC+ and BD+, and especially a low-frequency component of the spectrum works on noise with regard to a tracking error signal. Further, in the case of a tracking error signal according to the DPD TE method, the magnitude and gain are reduced as track density is increased, which makes the accurate control of tracking in a high track- density structure difficult.

[0022] In order to improve such drawbacks, a tracking error detecting method according to the present invention involves generating clock signals synchronized with each of the binarized signals AC+ and BD+, to detect a phase difference between those clock signals. In this case, all pulses in the synchronized clock signals have the phase difference components of AC+ and BD+, so that a tracking error signal can be generated regardless of the lengths of pits or marks recorded on a disk.

[0023] Specifically, at the outset, outputs of optical detectors which are disposed along a diagonal line from a track center are each binarized. Secondly, clock signals synchronized with each of the outputs obtained from the binarization are generated by PLL circuits. When a laser spot deviates from a track center, the outputs AC+ and BD+ obtained from the binarization have a phase difference corresponding to the deviation degree of the laser spot with regard to the track center, and the clocks which are phase locked to the outputs have the same phase difference. Thirdly, a phase difference between the synchronized clock signals output in the phase locking is detected. All clocks in the synchronized clock signals have the phase difference components of AC+ and BD+, so that a phase difference component is detected on a clock-by-clock basis. Lastly, the output from the phase difference detection is filtered by an LPF to obtain a tracking error signal.

[0024] Figure 3 is a block diagram showing a first preferred embodiment of a tracking error detecting apparatus according to the present invention. The apparatus shown in Figure 3 includes a four-section optical detection unit 302, a matrix circuit 304, equalizers (EQs) 306a and 306b, binarizers 308a and 308b, PLLs 310a and 310b, a phase comparator 312, LPFs 314a and 314b, a differential amplifier 316, and a frequency divider 318.

[0025] The matrix circuit 304 for adding optical detection signals A and C, and B and D among the outputs A, B, C and D of the four-section optical detection unit 302, turns the outputs AC1 and BD1 into A+C and B+D, respectively. That is, the matrix circuit 304 produces summation signals of the signals generated by optical detectors which are positioned along a diagonal line from a track center. The EQs 306 a and 306b for strengthening the high-frequency components of AC1 and BD1 provided from the matrix circuit 304 and removing noise therefrom, differentiate AC1 and BD1 and remove noise therefrom to output the results AC2 and BD2 to the binarizers 308a and 308b. In other words, since the outputs A, B, C and D of the four-section optical detection unit 302 have weak high-frequency components, the high-frequency components of AC1 and BD1 provided from the matrix circuit 304 are reinforced through the EQs 306a and 306b. Further, as the outputs A, B, C and D of the four-section optical detection unit 302 contain a noise component in addition to signals reflected from an optical disk, EQs 306a and 306b eliminate the noise component in AC1 and BD1 provided from the matrix circuit 304.

[0026] The binarizers 308a and 308b for converting AC2 and BD2 provided from EQS 306a and 306b into binary digital signals binarize AC2 and BD2 to output the results AC3 and BD3 to the PLLs 310a and 310b. Through the binarizers 308a and 308b, binarization level compensation for AC2 and BD2 provided from the EQS 306a and 306b can be performed. The PLLs 310a and 310b for generating clock signals (CLKs) synchronized with AC3 and BD3 which are provided from the binarizers 308a and 308b accept the input signals CLK, AC3 and BD3 and output CLK_AC and CLK_BD, synchronized with AC3 and BD3, to the phase comparator 312. The phase comparator 312 for detecting a phase difference between CLK_AC and CLK_BD, provided from the PLLs 310a and 310b, compares the phases of CLK_AC and CLK_BD to output the results AC+ and BD+ to LPFs 314a and 314b, respectively. In this case, AC+ and BD+ are phase difference signals generated when CLK_AC leads CLK_BD in phase and when CLK_BD leads CLK_AC in phase, respectively.

[0027] The LPFs 314a and 314b filter AC+ and BD+ provided from the phase comparator 312 to output the results to the differential amplifier 316. The differential amplifier 316 amplifies the difference signal of AC+ and BD+ filtered by the LPF5 314a and 314b to output the result as a tracking error signal (TE).

[0028] Figure 4 is a wave form diagram showing the operation of the apparatus shown in Figure 3. In Figure 4 showing the case in which AC3 leads BD3 in phase, the wave forms of AC3, BD3, CLK_AC, CLK_BD, AC+, and BD+ signals are illustrated sequentially from the top. As shown in Figure 4, it can be found that if a laser spot deviates from a track center by a predetermined amount, a phase difference existing between AC3 and BD3 is transferred to CLK_AC and CLK_BD, doubling

by a CLK frequency. Figure 4 indicates that CLK_AC and CLK_BD synchronized with AC3 and BD3 respectively are generated and a phase difference Δt created between AC3 and BD3 is transferred to the outputs CLK_AC and CLK_BD of the PLLs 310a and 310b. Thus, the phase difference value Δt can be derived as a result of comparing the phases of CLK_AC and CLK_BD.

[0029] The conventional apparatus detects the phase difference Δt once in an interval t1, while the apparatus according to embodiments of the present invention can detect the phase difference Δt once every CLK cycle. When a channel clock is used as CLK, the phase difference Δt can be detected once every channel clock cycle T regardless of the lengths of pits or marks recorded on an optical disk. The frequency divider 318 frequency divides CLK at an interval where inversion of the output signal takes place, to output the result to the PLLs 310a and 310b. In the apparatus of Figure 3, a tracking servo control becomes unstable at the interval where inversion of the output signal happens. This is because inversion of the output signals causes deviation from the extent of phase difference detection by the PLLs 310a and 310b. Thus, in order to compensate for the deviation, the frequency of CLK is divided at the interval where inversion of the output signal occurs and the result is provided to the PLLs 310a and 310b.

[0030] Figure 5 is a block diagram showing a second embodiment of a tracking error detecting apparatus according to the present invention. The apparatus shown in Figure 5 includes a four-section optical detection unit 502, EQs 506a-506d, binarizers 508a-508d, PLLs 510a-510d, phase comparators 512a and 512b, LPFs 514a-514d, differential amplifiers 516a and 516b, and an adder 518. Since outputs A, B, C and D of the four-section optical detection unit 302 have weak high-frequency components, the high-frequency component of A, B, C and D provided from the four-section optical detection unit 502 is reinforced through the EQs 506a-506d. Further, as the outputs A, B, C and D of the four-section optical detection unit 302 contain noise in addition to signals reflected from an optical disk, EQs 506a-506d eliminate the noise components of A, B, C and D provided from the four-section optical detection unit 502.

[0031] The binarizers 508a-508d for converting signals provided from EQs 506a-506b into binary digital signals binarize those signals to output the results to the PLLs 510a-510d. The PLLs 510a-510d for generating CLKs synchronized with the signals which are provided from the binarizers 508a-508d receive as input CLK and the signals provided from the binarizers 508a-508d to output CLKs synchronized with each of the signals provided from the binarizers 508a-508d to the phase comparators 512a and 512b. The phase comparators 512a and 512b are for detecting phase differences between CLK_A and CLK_B and between CLK_C and CLK_D provided from the PLLs 510a-510d. The phase comparator 512a compares the phases of CLK_A and CLK_B to output the results A+ and B+ to the LPFs 514a and 514b, respectively, while the phase comparator 512b compares the phases of CLK_C and CLK_D to output the results C+ and D+ to the LPFs 514c and 514d, respectively. In this case, A+ and B+ are phase difference signals generated when CLK_A leads CLK_B in phase and when CLK_B leads CLK_A in phase, respectively. Further, C+ and D+ are phase difference signals generated when CLK_C leads CLK_D in phase and when CLK_D leads CLK_C in phase, respectively.

[0032] The LPFs 514a-514d filter A+, B+, C+ and D+ provided from the phase comparators 512a and 512b to output the results to the differential amplifiers 516a and 516b. The differential amplifiers 516a and 516b amplify the difference signals of A+ and B+, and C+ and D+ filtered by the LPFs 514a to 514d to output the results to the adder 518. The adder for adding signals provided from the differential amplifiers 516a and 516b adds those signals to output the result as TE.

[0033] Figure 6 is a block diagram showing a third preferred embodiment of a tracking error detecting apparatus according to the present invention, in which TE is produced using outputs of a three-section optical detection unit. The apparatus shown in Figure 6 includes a three-section optical detection unit 602, EQs 606a and 606b, binarizers 608a and 608b, PLLs 610a and 610b, a phase comparator 612, LPFs 614a and 614b, and a differential amplifier 616.

[0034] The EQs 606 a and 606b for strengthening the high-frequency components of signals E and G provided from optical detectors disposed at the outside of the three-section optical detection unit 602 and removing noise therefrom, differentiate E and G and remove noise therefrom to output the results to the binarizers 608a and 608b. The binarizers 608a and 608b for converting the signals provided from EQs 606a and 606b into binary digital signals binarize those signals to output the results E3 and G3 to the PLLs 610a and 610b. The PLLs 610a and 610b for generating CLKs synchronized with the signals which are provided from the binarizers 608a and 608b receive as input CLK, E3 and G3 to output CLK_E and CLK_G synchronized with E3 and G3 to the phase comparator 612. The phase comparator 612 for detecting a phase difference between CLK_E and CLK_G provided from the PLLs 610a and 610b, compares the phases of CLK_E and CLK_G and outputs the results E+ and G+ to the LPFs 614a and 614b, respectively. In this case, E+ and G+ are phase difference signals generated when CLK_E leads CLK_G in phase and when CLK_G leads CLK_E in phase, respectively.

[0035] The LPFs 614a and 614b filter E+ and G+ provided from the phase comparator 612 to output the results to the differential amplifier 616. The differential amplifier 616 amplifies the difference signal of E+ and G+ filtered by the LPFs 614a and 614b to output the result as TE.

[0036] Figure 7 is a block diagram showing a fourth preferred embodiment of a tracking error detecting apparatus according to the present invention in which TE is produced using the output of a three-section optical detection unit. The apparatus shown in Figure 7 includes a three-section optical detection unit 702, EQs 706a and 706b, binarizers 708a and 708b, a phase comparator 712, LPFs 714a and 714b, and a differential amplifier 716.

[0037] The EQS 706a and 706b for strengthening the high-frequency components of signals E and G provided from optical detectors disposed at the outside of the three-section optical detection unit 702 and removing noise therefrom, differentiate E and G and remove noise therefrom to output the results to the binarizers 708a and 708b. The binarizers 708a and 708b for converting the signals provided from EQs 706a and 706b into binary digital signals binarize those signals to output the results E3 G3 to the phase comparator 712. The phase comparator 712 for detecting a phase difference between E3 and G3 provided from the EQs 706a and 706b, compares the phases of E3 and G3 to output the results E+ and G+ to the LPFs 614a and 614b, respectively. In this case, E+ and G+ are phase difference signals generated when E3 leads G3 in phase and when G3 leads E3 in phase, respectively.

[0038] The LPFs 714a and 714b filter E+ and G+ provided from the phase comparator 712 to output the results to the differential amplifier 716. The differential amplifier 716 amplifies the difference signal of E+ and G+ filtered by the LPFs 714a and 714b to output the result as TE.

[0039] Figure 8 is a graph showing operation of the EQs of Figure 3 and 5-7, in which the vertical axis and the horizontal axis indicate gain and frequency, respectively. The EQs having the properties as shown in Figure 8 perform the function of controlling their properties so that an input signal can be positioned between a first frequency f1 and a second frequency f2 to amplify the high-frequency component which is close to the second frequency f2.

[0040] Figure 9 is a graph showing the result of comparing a tracking error signal generated by a tracking error detecting apparatus according to the present invention with a tracking signal generated by a conventional DPD TE method. In Figure 9, reference numerals 91 and 92 respectively represent tracking error signals generated by a conventional DPD TE method and a tracking error detecting apparatus according to the present invention, and it can be seen that the gain of the latter is greater than that of the former. Further, an interval 93 indicates the section where inversion of output signal occurs so that a phase difference will exceed the detection limit if the phase difference is detected using the CLKs generated from the PLLs as in the present invention. If this is the case, the frequency of the PLL CLK can be divided by n (n=2,3,4,...) and the result is output to a phase difference detector, which increases the detection extent so that intervals such as 93 will not exist.

[0041] Figure 10 is a graph showing the characteristic of gain of tracking error signals generated by a tracking error detecting apparatus according to the present invention and a conventional DPD TE method. In Figure 10, reference numerals 94 and 95 respectively indicate the gains of tracking error signals generated by the conventional DPD TE method and the tracking error detecting apparatus according to the present invention. If both are measured under the same conditions, it can be seen that the gain of a tracking error signal generated in the apparatus according to the present invention is about 10 times greater than the gain of the other. An interval 96 is the section where an optical pickup jumps on an adjacent track in a normal tracking state. While the interval 96 cannot be shown clearly in a tracking error signal generated by the conventional DPD TE method, it is output as a large value in a tracking error signal generated by the present invention.

[0042] As described in the foregoing, a tracking error detecting apparatus according to the present invention is capable of generating a tracking error signal which does not vary depending on the lengths of pits and marks recorded on a optical disk, so that reliability of the tracking error signal can be enhanced.

[0043] While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention as defined in the appended claims.

[0044] The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

[0045] All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

[0046] Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

[0047] The invention is not restricted to the details of the foregoing embodiment(s). The invention extend to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. A tracking error detecting method for producing a tracking error signal as a difference signal of optical detection signals generated from more than two optical detectors positioned along a diagonal line from a track center, the method comprising the steps of:

   binarization for binarizing each of the outputs of the optical detectors;

   phase locking for generating clock signals synchronized with each of the outputs obtained by the binarization;

   phase difference detection for detecting a phase difference between the synchronized clock signals output from the phase locking; and

   low-pass filtering for filtering the output of the phase difference detection to output the result as the tracking error signal.

2. A tracking error detecting apparatus for producing a tracking error signal as a difference signal of optical detection signals generated from more than two optical detectors positioned along a diagonal line from a track center, the apparatus comprising:

   binarizers (308a, 308b; 508a, 508b, 508c, 508d; 608a, 608b) for binarizing each of the outputs of the optical detectors;

   phase locked loops (310a, 310b; 510a-d; 610a, 610b) for generating clock signals synchronized with each of the outputs of the binarizers (308a, 308b; 508a, 508b, 508c, 508d; 608a, 608b);

   a phase difference detector (312; 512a, 512b; 612) for detecting a phase difference between the synchronized clock signals output from the phase locked loops (310a, 310b; 510a-d; 610a, 610b) ; and

   a low-pass filter (314a, 314b; 514a-d; 614a, 614b) for filtering the output of the phase difference detector (312; 512a, 512b; 612) to output the result as the tracking error signal.

3. The tracking error detecting apparatus of claim 2, further comprising equalizers (306a, 306b; 506a-d; 606a, 606b) for reinforcing the high-frequency components of the outputs of the optical detectors to output the result to the binarizers (308a, 308b; 508a-d; 608a, 606b).

4. The tracking error detecting apparatus of claim 3, wherein the equalizers (306a, 306b; 506a-d; 606a, 606b) remove low-frequency components of a spectrum from the outputs of the optical detectors (302; 502; 602), according to a recording modulation method.

5. The tracking error detecting apparatus of claim 2, 3 or 4, wherein a clock signal provided to the phase locked loops (310a, 310b; 510a-d; 610a, 610b) is a channel clock signal.

6. The tracking error detecting apparatus any of claims 2 to 5, further comprising a frequency divider (318) for dividing the frequency of the channel clock signal by n (n=2,3,4,...) to output the result to the phase locked loops when the phase of an output signal is inverted.

7. The tracking error detecting apparatus of any of claims 2 to 6, wherein the phase difference detector (312; 512a, 512b; 612) generates a first phase difference signal indicating that a first synchronized clock signal output from the phase locked loops leads a second synchronized clock signal output from the phase locked loops, and a second phase difference signal indicating that the second synchronized clock signal leads the first synchronized clock signal, and

   wherein the low-pass filters (314a, 314b; 514a-d; 614a, 614b) include first and second low-pass filters for filtering the first and second phase difference signals, respectively.

8. The tracking error detecting apparatus of any of claims 2 to 7, further comprising a differential amplifier (316; 516a, 516b, 518; 616) for generating a tracking error signal corresponding to a difference signal of the outputs of the first and second low-pass filters (314a, 314b; 614a, 614b).

9. A tracking error detecting apparatus for producing a tracking error signal as a difference signal of optical detection signals generated from two optical detectors disposed at the outside of the track center of a three-section optical detection unit, the apparatus comprising:

   binarizers (308a, 308b; 508a-d; 608a, 608b; 708a, 708b) for binarizing each of the outputs of the two optical detectors;

   a phase difference detector (312; 512a, 512b; 612; 712) for detecting a phase difference between the outputs of the binarizers (308a, 308b; 508a-d; 608a, 608b; 708a, 708b); and

   a low-pass filter (314a, 314b; 514a-d; 614a,

614b; 714a, 714b) for filtering the output of the phase difference detector to output the result as the tracking error signal.

10. The tracking error detecting apparatus of claim 9, further comprising phase locked loops (310a, 310b; 510a-d; 610a, 610b) coupled to the binarizers (308a, 308b; 508a-d; 608a, 608b) and the phase difference detector (312; 512a, 512b; 612), which are for generating clock signals synchronized with each of the outputs of the binarizers (308, 308b; 508a-d; 608a, 608b) to output the synchronized signals to the phase difference detector, (312; 5123a, 512b; 612)

    wherein the phase difference detector (312; 512a, 512b; 612) detects a phase difference between the synchronized signals output from the phase locked loops (310a, 310b; 510a-d; 610a, 610b).

FIG. 1 (PRIOR ART)

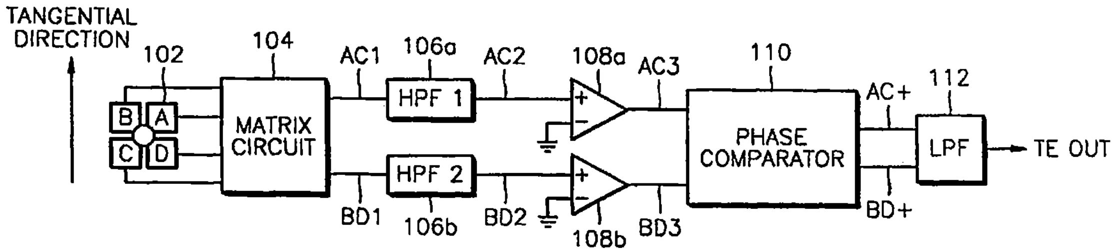


FIG. 2 (PRIOR ART)

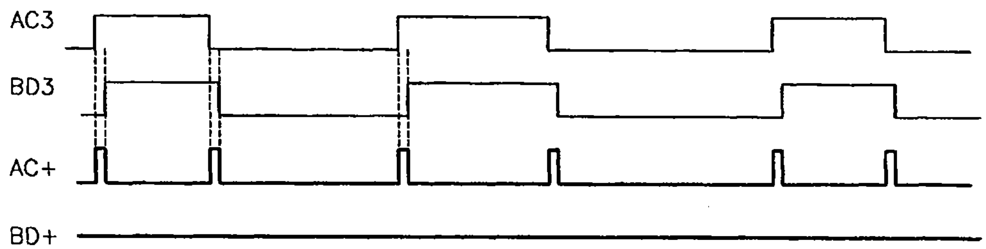
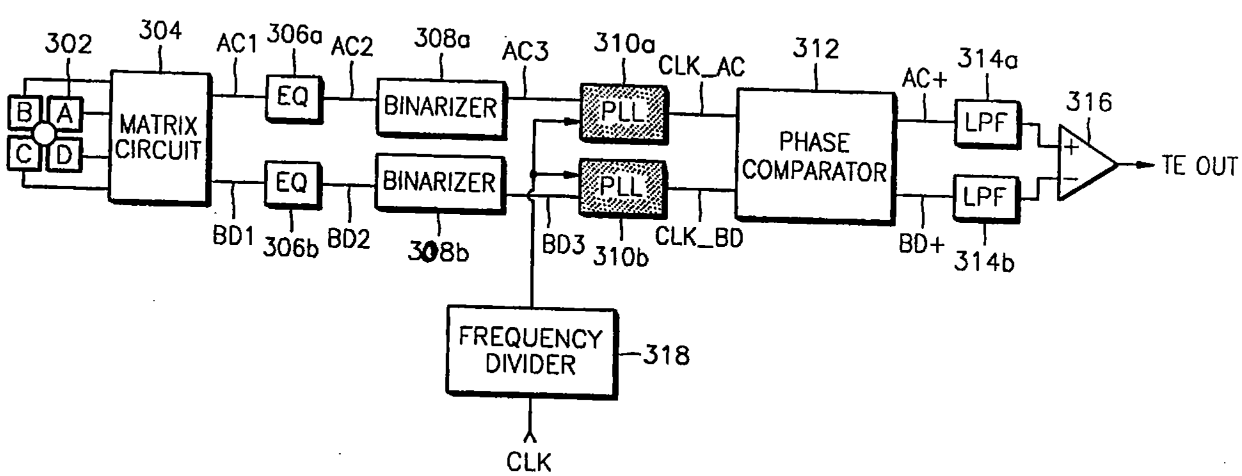
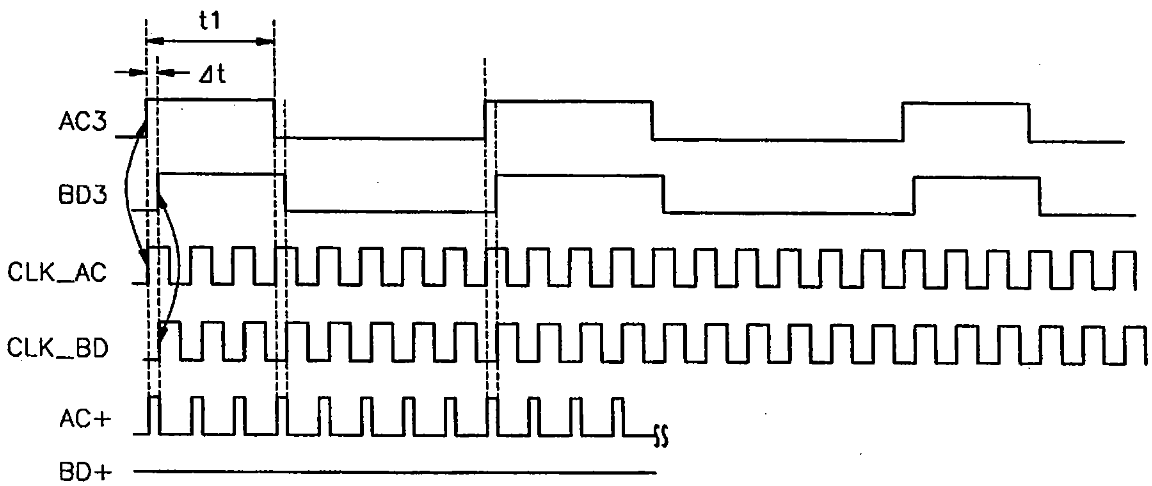


FIG. 3



EP 1 067 525 A2

FIG. 4



EP 1 067 525 A2

FIG. 5

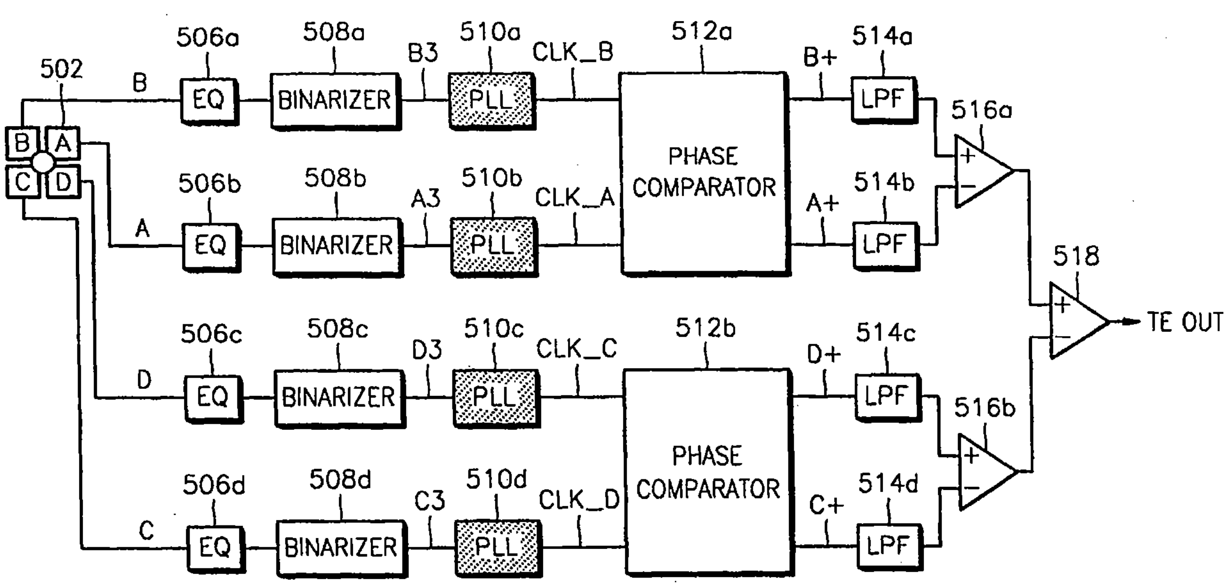


FIG. 6

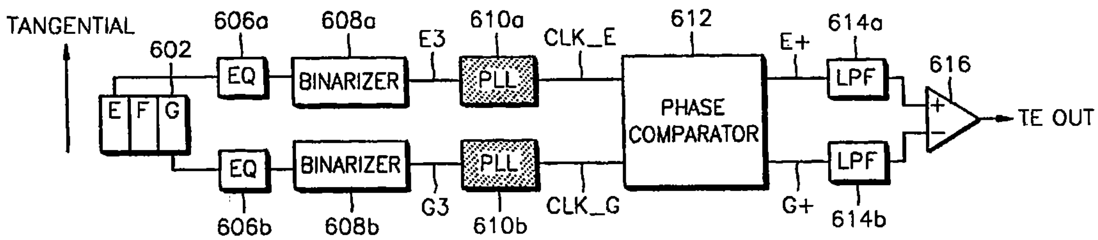
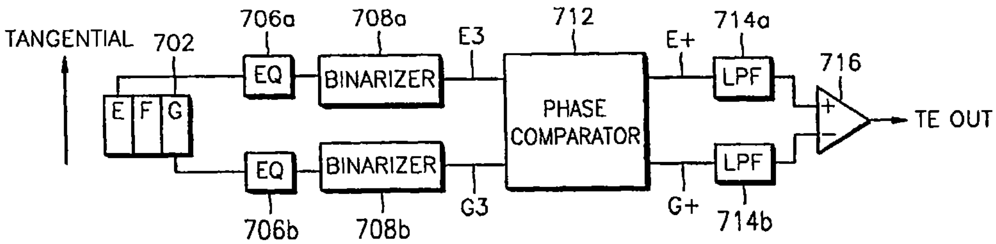


FIG. 7



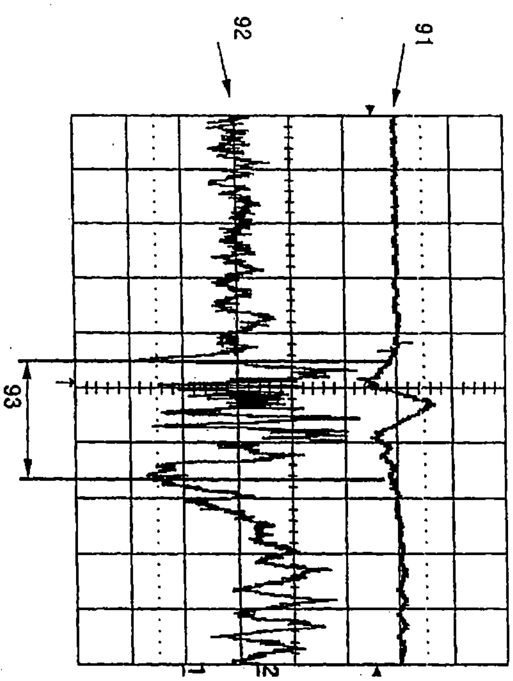


FIG. 9

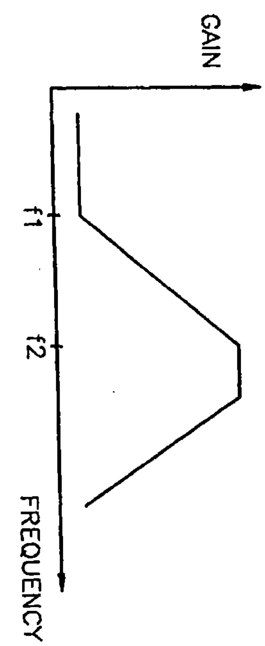


FIG. 8

FIG. 10